**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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AF

Applicant: Suresh Marisetty et al.

Title: ERROR CORRECTION APPARATUS, SYSTEMS, AND METHODS

Docket No.: 884.108US2
Filed: July 28, 2003
Examiner: Michael C. Maskulinski

Serial No.: 10/628,726
Due Date: December 6, 2005
Group Art Unit: 2113


**MS Appeal Brief - Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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X APPELLANTS' BRIEF ON APPEAL including Appendices (27 pgs.).
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By: Ann M. McCrackin
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CAROLYN HULSEY
Name

Carolyn Hulsey
Signature

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| Applicant: | Suresh Marisetty et al. | Examiner: | Michael C. Maskulinski |
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| Assignee: | Intel Corporation | Customer Number: | 21186 |

## APPELLANTS' BRIEF ON APPEAL

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, mailed on October 6, 2005, from the Final Rejection of claims 5-19 and 24-26 of the above-identified Application, as set forth in the Final Office Action mailed on July 6, 2005, and the Advisory Action mailed on September 15, 2005.

The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of $500.00 which represents the requisite fee set forth in 37 C.F.R. § 41.2(b)(2). The Appellant respectfully requests consideration and reversal of the Examiner's rejections of the pending claims.

## TABLE OF CONTENTS

## 1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, INTEL CORPORATION.

## 2. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings known to the Appellant that will have a bearing on the Board's decision in the present appeal.

## 3. STATUS OF THE CLAIMS

The present Application was filed on July 28, 2003 with claims 1-26, as a divisional of U.S. Patent Application Serial No. 09/405,972, filed September 27, 1999, now issued as U.S. Patent No. 6,675,324. After one Non-Final Office Action and a Final Office Action (hereinafter "the Final Office Action") were received, and timely responses filed thereto, an Advisory Action was mailed on September 15, 2005 (hereinafter "the Advisory Action").

At this time, claims 1-26 are currently pending in the Application. Claims 1-4 and 21-23 have been allowed. An objection has been raised with respect to claim 20 as being dependent on rejected base claims. Claims 5-19 and 24-26 stand rejected, and their rejection is appealed herein.

## 4. STATUS OF AMENDMENTS

No amendments have been made subsequent to those proposed by the Appellant for claims 17, 20, 24, and 26 in the response to the Final Office Action. However, these amendments were not entered by the Examiner in the Advisory Action. The Appellant has therefore not indicated the amendments in the Claims Appendix attached hereto. As noted in the response to the Final Office Action, none of the amendments was made for reasons related to patentability.

## 5. SUMMARY OF CLAIMED SUBJECT MATTER

This summary is presented in compliance with the requirements of Title 37 C.F.R. § 41.37(c)(1)(v), mandating a "concise explanation of the subject matter defined in each of the independent claims involved in the appeal ...". Nothing contained in this summary is intended to change the specific language of the claims described, nor is the language of this summary to be construed so as to limit the scope of the claims in any way.

Some embodiments of the invention are related to a system comprising a non volatile memory to store an error handling routine and an idle routine (said error handling routine to permit a computer system to continue operating when an error is detected, a plurality of slave processors to execute the idle routine (wherein the plurality of slave processors are included in the computer system), and a monarch processor included in the computer system, the monarch processor being capable of executing the error handling routine to correct the error. (Application, Independent claim 5; FIGs. 1 and 5; pg. 4, lines 10-16; pg. 5, line 20 – pg. 10, line 7; and pg. 14, lines 15-19).

Some embodiments of the invention are related to a system comprising a plurality of processors including a monarch processor, a processor abstraction layer coupled to the plurality of processors, a system abstraction layer coupled to the processor abstraction layer, an operating system layer coupled to the system abstraction layer, and an interrupt signaling mechanism coupled to the processor abstraction layer, the system abstraction layer, and the operating system layer to initiate a rendezvous state and to end the rendezvous state, said rendezvous state being a state where all of the plurality of processors but the monarch processor are idle. (Application, Independent claim 8; FIGs. 1, 2, 3, and 5; pg. 4, lines 10-16; pg. 5, line 20 – pg. 12, line 31; and pg. 14, lines 15-19).

Some embodiments of the invention are related to a system comprising a plurality of processors, a processor abstraction layer located in a non volatile memory coupled to the plurality of processors, a system abstraction layer located in the non volatile memory, and an operating system layer located in a system memory coupled to the plurality of processors to signal all but one of the plurality of processors to end a rendezvous state upon receiving a signal that error handling is completed, said rendezvous state being a

state wherein all but the one of said plurality of processors are idle. (Application, Independent claim 12; FIGs. 2, 3, and 5; pg. 4, lines 10-16; pg. 10, line 8 – pg. 12, line 31; and pg. 14, lines 15-19).

Some embodiments of the invention are related to a method comprising detecting an error by one processor included in a multiple processor system, entering a rendezvous state in which all processors but the one processor included in the multiple processor system are idle, correcting the error using the one processor, and resuming normal operation. (Application, Independent claim 15; FIGs. 4 and 5; and pg. 13, line 1 – pg. 14, line 19).

Some embodiments of the invention are related to a method comprising attempting to correct an error by a detecting processor included in a multiple processor system, on failure, executing firmware code operatively coupled to all the processors included in the multiple processor system to correct the error, and on failure, entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of the processors included in the multiple processor system are idle. (Application, Independent claim 18; FIGs. 1-3 and 5; pg. 5, line 20 – pg. 12, line 31; and pg. 14, lines 15-19).

Some embodiments of the invention are related to a method comprising attempting to correct an error by a processor included in a plurality of processors, accessing a routine in a first firmware layer to correct the error, selecting a monarch processor included in the plurality of processors, executing a spin loop routine in a second firmware layer by the plurality of processors except the monarch processor, accessing a routine in the second firmware layer to correct the error, and resuming normal operation by the plurality of processors. (Application, Independent claim 21; FIGs. 1, 2, and 5; pg. 5, line 20 – pg. 11, line 26; and pg. 14, lines 15-19).

Some embodiments of the invention are related to an article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing the activities of attempting to correct an error by a detecting processor included in a multiple processor system, on failure, executing firmware code operatively coupled to all the processors included in the multiple

processor system to correct the error, and on failure, entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of the processors included in the multiple processor system are idle. (Application, Independent claim 24; FIGs. 2 and 5; pg. 4, lines 10-16; pg. 10, line 8 – pg. 11, line 26; and pg. 14, lines 15-19).

## 6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

**6.1** Claims 24-26 stand rejected under 35 USC § 101 as being directed to non-statutory subject matter.

**6.2** Claims 5-16 and 24-26 stand rejected under 35 USC § 102(b) as being anticipated by Bowers (U.S. 6,308,285 B1; hereinafter "Bowers").

**6.3** Claims 18 and 19 stand rejected under 35 USC § 102(e) as being anticipated by Falik et al. (U.S. 6,065,078; hereinafter "Falik").

**6.4** Claim 17 stands rejected under 35 USC § 103(a) as being unpatentable over Bowers and further in view of Fujii et al. (U.S. 5,892,898; hereinafter "Fujii").

## 7. ARGUMENT

### *7.1 The Applicable Law*

With respect to 35 USC § 101, the court in *Alappat* noted that the "... plain and unambiguous meaning of section 101 is that any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may be patented if it meets the requirements for patentability set forth in Title 35, such as those found in sections 102, 103, and 112. The use of the expansive term "any" in section 101 represents Congress's intent not to place any restrictions on the subject matter for which a patent may be obtained beyond those specifically recited in section 101 and the other parts of Title 35.... Thus, it is improper to read into section 101 limitations as to the subject matter that may be patented where the legislative history does not indicate that Congress clearly intended such limitations." *In re Alappat*, 33 F.3d at 1542, 31 USPQ2d 1545, 1556 (Fed. Cir. 1994) (en banc).

The AT&T court stated that the "... scope of 35 U.S.C. § 101 is the same regardless of the form or category of invention in which a particular claim is drafted. *AT&T*, 172 F.3d at 1357, 50 USPQ2d at 1451 . *See also State Street*, 149 F.3d at 1375, 47 USPQ2d at 1602.

Further, "Alappat admits that claim 15 would read on a general purpose computer programmed to carry out the claimed invention, but argues that this alone also does not justify holding claim 15 unpatentable as directed to nonstatutory subject matter. We agree. We have held that such programming creates a new machine, because a general purpose computer in effect becomes a special purpose computer once it is programmed to perform particular functions pursuant to instructions from program software. . . . The Supreme Court has never held that a programmed computer may never be entitled to patent protection. . . . Consequently, a computer operating pursuant to software may represent patentable subject matter, provided, of course, that the claimed subject matter meets all of the other requirements of Title 35." *In re Alappat* at 1558.

Next, it is respectfully noted that anticipation under 35 USC § 102 requires the disclosure in a single prior art reference of each element of the claim under consideration.

*See Verdegaal Bros. V. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131 (emphasis added).

Finally, the Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). In combining prior art references to construct a *prima facie* case, the Examiner must show some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art that would lead an individual to combine the relevant teaching of the references. *Id.* The M.P.E.P. contains explicit direction to the Examiner that agrees with the *In re Fine* court:

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Appellant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

An invention can be obvious even though the suggestion to combine prior art teachings is not found in a specific reference. *In re Oetiker*, 977 F.2d 1443, 24 U.S.P.Q.2d (BNA) 1443 (Fed. Cir. 1992). However, while it is not necessary that the cited references or prior art specifically suggest making the combination, there must be some teaching somewhere which provides the suggestion or motivation to combine prior

art teachings and applies that combination to solve the same or similar problem which the claimed invention addresses.

One of ordinary skill in the art will be presumed to know of any such teaching. (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7 U.S.P.Q.2d 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599 F.2d 1032, 1037, 202 U.S.P.Q. 171, 174 (C.C.P.A. 1979)). However, the level of skill is not that of the person who is an innovator but rather that of the person who follows the conventional wisdom in the art. *Standard Oil Co. v. American Cyanamid Co.,* 774 F.2d 448, 474, 227 U.S.P.Q. 293, 298 (Fed. Cir. 1985). The requirement of a suggestion or motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which notes that the motivation must be supported by evidence in the record.

### *7.2 The References*

***Bowers:*** teaches a scheme to replace one or more processors in a multiprocessor computer without rebooting the system. (Col. 2, lines 49-63). An interrupt generated as a result of user activity, either by execution of a utility program, or flipping a switch, is used to signal a controller (programmable array logic) that a processor is to be replaced. (Col. 4, lines 29-43). The controller operates to place all processors into a sleep mode. (Col. 2, line 53). A _PTS routine stores information in a non-volatile memory and signals the programmable array logic to generate stop clock STPCLK# and sleep SLP# signals, which are in turn delivered to each processor. (Col. 4, line 60 - Col. 5, line 9). The processor to be replaced is then disconnected from power, replaced, configured, and put to sleep before waking up all processors in the system. (Col. 4, lines 17-25).

***Falik:*** speaks to a debugger interface, including separate circuitry, to interact with a plurality of processors. (Col. 1, lines 34-36). Debugger commands are directed to a selected processor, and processor commands are directed to the debugger. (Col. 1, lines 36-46). Messages are sent to processors in an RX session, wherein a selected processor is halted to execute a monitor routine capable of accessing the message to be received. (Col. 4, lines 30-46). A full system stop is used to observe the entire system status at

breakpoints. (Col. 5, lines 4-8). Erroneous conditions are cured by a system reset. (Col. 18, lines 31-48).

***Fujii:*** discloses an error event management system. (Col. 2, lines 1-19). Information, warnings, and errors are logged with the assistance of a service routine. (Col. 3, lines 55-63). An event viewer is used to observe the recorded information at a later time. (Col. 2, lines 53-56 and Col. 3, lines 23-30).

### *7.3 Discussion of the Rejection Under § 101:*

Claims 24-26 were rejected under 35 USC § 101 because it is alleged that the claimed invention is directed to non-statutory subject matter. The Final Office Action states that "[c]laim 24 claims a recording medium on which a program is stored and variations thereof. These claims are therefore interpreted as recording a program per se ... language, specifically stating [sic] the claim, **must be** limited to a computer program stored on a computer recordable medium executing on a computer." [emphasis in original] The Appellant respectfully disagrees.

In view of the Court's ruling in *Alappat* and *AT&T*, it is respectfully noted that claims 24-26 recite the structure of "[a]n article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing ...". These claims are therefore directed to an article of manufacture, including a system 500 executing code stored in a system memory 540 (see page 14 of the Application, lines 15-16), and as such, clearly fall into one of the four acceptable statutory categories of patentable subject matter. Further, the subject matter of claims 24-26 also clearly conforms to the requirements of the "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility" promulgated by the United States Patent Office on October 26, 2005. The Appellant therefore respectfully requests that the rejection of claims 24-26 under 35 USC § 101 be reconsidered and withdrawn.

### *7.4 Discussion of the Rejections Under § 102:*

Claims 5-16 and 24-26 were rejected under 35 USC § 102(b) as being anticipated by Bowers. Claims 18 and 19 were rejected under 35 USC § 102(e) as being anticipated by Falik. First, the Appellant does not admit that Bowers or Falik are prior art, and reserves the right to swear behind these references in the future. Second, since neither Bowers nor Falik anticipate each and every element of the invention as claimed by the Appellant, these rejections under 35 U.S.C. § 102 are respectfully traversed.

As admitted by the Office, the sleep signal SLP# of Bowers is "delivered to *each* processor" such that "all processors are placed into a sleep mode." *See* Office Action, Mail Date 20050128, pg. 4, lines 6-8 and Bowers, Col. 2, line 53. This method of operation by Bowers is further supported by the Office admission that "The processors also stop executing commands ...". *Id.* at pg. 4, line 10. That is, Bowers uses a controller (programmable array logic) to put each and every processor in the system to sleep, which is necessary, because this operation permits any one of the processors in Bowers to be physically replaced. *See* Bowers, Col. 2, lines 53-56. As a matter of contrast, in the embodiments claimed by the Appellant, one processor taken from the plurality of processors (e.g., the monarch processor) remains awake while other processors are put to sleep.

Given the method of operation disclosed in Bowers, the Office Action rejects the instant claims by attempting to characterize Bowers' controller as a "monarch processor." However, this is inappropriate. First, because Bowers makes a clear distinction between the "controller" and the "processors." It is *only* the controller in Bowers, and not the processors, that can access data used to put the processors to sleep. Second, even if one accepts the premise that Bowers' controller can operate as a monarch processor, the conclusion would be that Bowers' controller, as one of the plurality of processors, could also be put to sleep for replacement as directed by one of the other processors in Bowers' system. This type of operation, claimed by the Appellant, is not possible using Bowers' system.

Therefore, Bowers does not teach or suggest a "monarch processor being capable of executing the error handling routine to correct the error ..." as claimed by the Appellant in independent claim 5 (and dependent claims 6-7) such that "the monarch processor is capable of sending a wake up signal to the plurality of slave processors to exit the rendezvous state" as claimed in claim 7.

Further, Bowers does not teach or suggest "a plurality of processors including a monarch processor ... and an interrupt signaling mechanism ... to initiate a rendezvous state ... being a state where all of the plurality of processors but the monarch processor are idle" as claimed by the Appellant in independent claim 8 (and dependent claims 9-11). In addition, Bowers does not teach or suggest "a plurality of processors ... and an operating system layer ... to signal all but one of the plurality of processors to end a rendezvous state ... upon receiving a signal that error handling is completed, said rendezvous state being a state wherein all but the one of said plurality of processors are idle" as claimed by the Appellant in independent claim 12 (and dependent claims 13-15).

Bowers also does not teach or suggest "detecting an error ...; entering a rendezvous state in which all processors but the one processor included in the multiple processor system are idle; ... and ... correcting the error using the one processor" as claimed by the Appellant in independent claim 15 (and dependent claims 16-17). Finally, Bowers does not teach or suggest "attempting to correct an error ... in a multiple processor system ... and on failure, entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of the processors included in the multiple processor system are idle" as claimed by the Appellant in claim 24 (and dependent claims 25-26).

Falik suffers from similar deficiencies. Specifically, Falik fails to disclose "attempting to correct an error by a detecting processor included in a multiple processor system" and "entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of the processors included in the multiple processor system are idle" as claimed in claims 18 and 19. While the Office Action asserts that Falik's debugger interface is somehow equivalent to a "detecting processor included in a multiple processor system", this does not comport with the clear distinction Falik makes

between the host computer 1820 and the multiprocessor integrated circuit 1810. *See* Falik, Col. 2, lines 37-40 and FIG. 18. Even if it is assumed that Falik's debugger can operate as a "detecting processor", how does Falik's system correct the error? Falik's debugger, or a monitor, are the only resources available, and neither one operates to "correct" the error. It is respectfully noted that the term "error" appears only once in Falik, concerning bus communication error probability. However, such errors are not processed by Falik's system. *See* Falik, Col. 18, lines 31-32. In fact, Falik states that, while such errors can be cured by a system reset, such operation should be "avoided by the host" since this resets the entire chip. *See* Falik, Col. 18, lines 39-47.

The Appellant agrees that the term debug, by definition, may include correcting logical or syntactical errors. However, there mere fact that debugging activity occurs does not mandate any particular agency by which the actions are accomplished. For example, debugging typically occurs using human decision processes to propose and test solutions. This is not the same as what is claimed by the Appellant, where the a detecting processor itself can operate by "attempting to correct an error ...". This type of activity is not disclosed by Falik.

Finally, how can "all but one of the processors included in the multiple processor system" be idle, as asserted in the Office Action, if at least one processor in Falik's multiprocessor integrated circuit 1810 must be awake to execute a monitor, *in addition* to the processor running the debugger on the host computer? The debugger communicates with the monitor on one of the processors, which means at least *two* processors must be operational to debug programs in Falik's system. See Falik, Col. 17, lines 27-46. This is not what is claimed by the Appellant.

In short, what is disclosed by Bowers and Falik is not identical to what is claimed by the Appellant, and therefore, the rejection under § 102 is improper. Reconsideration and allowance of claims 5-16, 18-19, and 24-26 is respectfully requested.

### *7.5 Discussion of the Rejections Under § 103:*

Claim 17 was rejected under 35 USC § 103(a) as being unpatentable over Bowers, in view of Fujii. First, the Appellant does not admit that Fujii is prior art, and reserves

the right to swear behind this reference in the future. Second, because a *prima facie* case of obviousness has not been established, the Appellant respectfully traverses this rejection under 35 U.S.C.§103(a).

First, there is no motivation to combine Bowers and Fujii. Bowers never uses the term "error", or discloses any type of error detection or handling routine. Processor boards are simply replaced after the fact – notably, for routine maintenance. *See* Bowers, Col. 4, lines 29-34. Similarly, Fujii never mentions removing a processor from a system.

Second, the Office mischaracterizes the claimed "severe error" (which causes entry into a rendezvous state) as being the same as the "non-recoverable problem" documented by Fujii. However, this characterization does not comport with the concept of a "rendezvous state" claimed by the Appellant:

> "An example of this type of error is a parity error in the processor instruction cache. In this case, firmware will invalidate the entire instruction cache, access another copy of the instruction, and resume execution of the interrupted process. This type of error can be signaled to a processor by the platform via a double bit ECC error on the system bus. This type of error is generally corrected by entering the rendezvous state." Application, pg. 7, lines 19-24.

Thus, contrary to the assertion in the Office Action, it would not have been obvious to "make the modification because an error event type is used to report a non-recoverable problem ... and a warning event type is used to indicate some kind of recoverable anomaly ... [k]nowing the severity of the event determines what action should be taken (removal of a processor)." Final Office Action, pg. 13, line 18. That is, the instant invention contemplates a recoverable error as a reason to enter the rendezvous state, not a non-recoverable one.

Third, it is not necessarily true that "knowing the severity of the event determines what action should be taken (e.g., removal of a processor)" as asserted in the Office Action. Errors of varying severity can occur within a computer system, and knowledge of the severity (e.g., non-recoverable) will not always be determinative as to whether a processor should be replaced (e.g. a main memory failure may be the culprit, or a hard disk failure, etc.). Since there is no evidence in the record to support the Office Action

assertion, the explicit requirements set forth by *In re Sang Su Lee* are not satisfied. Therefore, the Examiner appears to be using personal knowledge, and is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

Fourth, it should be noted that neither Bowers nor Fujii disclose using a processor that is part of a multi-processor system to correct an error within the system, as claimed by the Appellant (i.e., "detecting an error by one processor included in a multiple processor system; entering a rendezvous state in which all processors but the one processor included in the multiple processor system are idle; [and] correcting the error using the one processor" in claim 15, from which 17 depends). Thus, no combination of Bowers and Fujii can provide this element.

Fifth, combining Bowers with Fujii gives no reasonable expectation of success. Fujii merely teaches the existence of an error recording system, not a system to correct errors. The mechanism of replacing a processor (as taught by Bowers) in response to recording non-recoverable errors, advocated in the Office Action, also may not have any effect on solving the actual problem (e.g., a main memory failure, or a cache failure).

Since there is no motivation to combine the references, since no combination of the references can be made which teaches the claimed invention, and since combination gives no reasonable expectation of success, no *prima facie* case of obviousness has been established, and the Appellant respectfully requests reconsideration and withdrawal of the rejection with respect to claim 17 under 35 U.S.C. §103.

## 8. SUMMARY

It is respectfully submitted that no *prima facie* case of the existence of nonstatutory subject matter under 35 U.S.C. §101, nor of anticipation under 35 U.S.C. §102, nor of obviousness under 35 U.S.C. §103 has been established by the Office. Therefore, it is respectfully requested that the rejections of claims 5-19 and 24-26 be reconsidered and withdrawn. The Appellant respectfully submits that all of the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Appellant's attorney, Mark Muller at (210) 308-5677, or the undersigned attorney at (612) 349-9592, to facilitate prosecution of this Application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SURESH MARISETTY ET AL.

By their Representatives,

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Date Nov. 29, 2005 By Ann M. McCrackin
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 29th day of November, 2005.

CAROLYN HULSEY
Name

Carolyn Hulsey
Signature

## CLAIMS APPENDIX

1. (Allowed) A system, comprising:

a non volatile memory in which is stored an error handling routine, said error handling routine to permit a computer system to continue operating when an error is detected; and

a plurality of processors included in the computer system, wherein each processor of the plurality is capable of accessing the error handling routine on detecting an error and signaling remaining processors of the plurality of processors to enter a rendezvous state.

2. (Allowed) The system of claim 1, wherein the error is only correctable by entering the rendezvous state.

3. (Allowed) The system of claim 1, further comprising a processor abstraction layer located in the non volatile memory, wherein the processor abstraction layer includes the error handling routine.

4. (Allowed) The system of claim 1, further comprising a system abstraction layer located in the non volatile memory, wherein the system abstraction layer includes the error handling routine.

5. (Rejected) A system, comprising:

a non volatile memory to store an error handling routine and an idle routine, said error handling routine to permit a computer system to continue operating when an error is detected;

a plurality of slave processors to execute the idle routine, wherein the plurality of slave processors are included in the computer system; and

a monarch processor included in the computer system, the monarch processor being capable of executing the error handling routine to correct the error.

6. (Rejected) The system of claim 5, wherein the error handling routine is included in a system abstraction layer.

7. (Rejected) The system of claim 5, wherein the monarch processor is capable of sending a wake up signal to the plurality of slave processors to exit the rendezvous state.

8. (Rejected) A system, comprising:

a plurality of processors including a monarch processor;

a processor abstraction layer coupled to the plurality of processors;

a system abstraction layer coupled to the processor abstraction layer;

an operating system layer coupled to the system abstraction layer; and

an interrupt signaling mechanism coupled to the processor abstraction layer, the system abstraction layer, and the operating system layer to initiate a rendezvous state and to end the rendezvous state, said rendezvous state being a state where all of the plurality of processors but the monarch processor are idle.

9. (Rejected) The system of claim 8, further comprising a system memory and a non volatile memory, wherein the operating system layer is located in the system memory and capable of being executed by the plurality of processors, the processor abstraction layer is located in the non volatile memory and is capable of being executed by the plurality of processors, and the system abstraction layer is located in the non volatile memory and is capable of being executed by the plurality of processors.

10. (Rejected) The system of claim 8, wherein the monarch processor is capable of executing an error handling routine included in the system abstraction layer upon initiation of the rendezvous state.

11. (Rejected) The system of claim 8, wherein the processor abstraction layer includes a functional module for error handling.

12. (Rejected) A system, comprising:

a plurality of processors;

a processor abstraction layer located in a non volatile memory coupled to the plurality of processors;

a system abstraction layer located in the non volatile memory; and

an operating system layer located in a system memory coupled to the plurality of processors to signal all but one of the plurality of processors to end a rendezvous state upon receiving a signal that error handling is completed, said rendezvous state being a state wherein all but the one of said plurality of processors are idle.

13. (Rejected) The system of claim 12, wherein the signal from the operating system to end the rendezvous state is an interrupt.

14. (Rejected) The system of claim 12, wherein the processor abstraction layer is capable of sending a signal to the system abstraction layer to enter the rendezvous state and performing error handling upon entering the rendezvous state.

15. (Rejected) A method, comprising:

detecting an error by one processor included in a multiple processor system;

entering a rendezvous state in which all processors but the one processor included in the multiple processor system are idle;

correcting the error using the one processor; and

resuming normal operation.

16. (Rejected) The method of claim 15, wherein entering the rendezvous state comprises:

requesting a plurality of processors included in the multiple processor system to enter an idle state; and

waiting until the plurality of processors have entered the idles state.

17. (Rejected) The method of claim 15, further comprising:

determining if the error is a severe error; and

only upon determining that the error is a severe error, entering the rendezvous state.

18. (Rejected) A method, comprising:

attempting to correct an error by a detecting processor included in a multiple processor system;

on failure, executing firmware code operatively coupled to all the processors included in the multiple processor system to correct the error; and

on failure, entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of the processors included in the multiple processor system are idle.

19. (Rejected) The method of claim 18, wherein entering a rendezvous state to correct the error comprises:

selecting a monarch processor from the processors included in the multiple processor system;

signaling slave processors included in the multiple processor system to execute a spin loop; and

correcting the error by the monarch processor.

20. (Objected To) The method of claim 19, wherein correcting the error by the monarch processor includes executing routines in a processor abstraction layer, a system abstraction layer, and an operating system.

21. (Allowed) A method, comprising:

attempting to correct an error by a processor included in a plurality of processors;

accessing a routine in a first firmware layer to correct the error;

selecting a monarch processor included in the plurality of processors;

executing a spin loop routine in a second firmware layer by the plurality of processors except the monarch processor;

accessing a routine in the second firmware layer to correct the error; and

resuming normal operation by the plurality of processors.

22. (Allowed) The method of claim 21, wherein selecting a monarch processor comprises determining which processor included in the plurality of processors can best correct the error.

23. (Allowed) The method of claim 21, further comprising:

determining whether the error is severe.

24. (Rejected) An article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing:

attempting to correct an error by a detecting processor included in a multiple processor system;

on failure, executing firmware code operatively coupled to all the processors included in the multiple processor system to correct the error; and

on failure, entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of the processors included in the multiple processor system are idle.

25. (Rejected) The article of claim 24, wherein the rendezvous state is a state wherein all but the one of the processors included in the multiple processor system are executing a spin loop.

26. (Rejected) The article of claim 24, wherein the data, when accessed, results in the machine performing:

informing a processor abstraction layer when all but the one of the processors included in the multiple processor system have entered the idle state.

# EVIDENCE APPENDIX

**NONE**

## RELATED PROCEEDINGS APPENDIX

No Related Proceedings are known to the Appellants' Representative.